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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	25	Application Number	10/666,930
		Filing Date	September 19, 2003
		First Named Inventor	Farnworth et al.
		Art Unit	2812
		Examiner Name	S. Isaac
		Attorney Docket Number	2269-5529US (02-0766.00/US)

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:

Claims Appendix

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm	TraskBritt, P.C.		
Signature	Jason P. Nixon		
Printed Name	Jason P. Nixon		
Date	April 12, 2007	Reg. No.	58,604

CERTIFICATE OF MAILING

Express Mail Label Number: EV826303990US

Date of Deposit: April 12, 2007

Person Making Deposit: Cat Bratton

PTO/SB/17 (12-04v2)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL for FY 2007

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500.00

Complete If Known	
Application Number	10/666,930
Filing Date	9/19/2003
First Named Inventor	Farnworth et al.
Examiner Name	S. Isaac
Art Unit	2812
Attorney Docket No.	2269-5529US (02-0766.00/US)

METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify) : _____

☒ Deposit Account Deposit Account Number: 20-1469 Deposit Account Name: TraskBritt, PC

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee($)	Fee($)	Fee($)	Fee($)	Fee($)	Fees Paid ($)
Utility	300	150	500	250	200	100	____
Design	200	100	100	50	130	65	____
Plant	200	100	300	150	160	80	____
Reissue	300	150	500	250	600	300	____
Provisional	200	100	0	0	0	0	____

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee($)		Fee Paid ($)
____	-20 or HP=	____	x	____	=	____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		Extra Claims		Fee($)		Fee Paid ($)
____	- 3 or HP=	____	x	____	=	____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
____	____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)	Fee Paid ($)
____	- 100 =	____	/ 50 =	____	(round up to a whole number) x		= ____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	____
Other (e.g., late filing surcharge) : Filing a Brief in Support of an Appeal	500.00

SUBMITTED BY

Signature	Jason P. Nixon	Registration No. (Attorney/Agent) 58,604	Telephone 801-532-1922
Name (Print/Type)	Jason P. Nixon		Date April 12, 2007

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Farnworth et al.

Serial No.: 10/666,930

Filed: September 19, 2003

For: METHOD FOR SUPPORTING WAFERS FOR DIE SINGULATION AND SUBSEQUENT HANDLING (as amended)

Confirmation No.: 6453

Examiner: S. Isaac

Group Art Unit: 2812

Attorney Docket No.: 2269-5529US

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EV826303990US

Date of Deposit with USPS: April 12, 2007

Person making Deposit: Cat Bratton

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Board of Patent Appeals and Interferences

Sirs:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal (hereinafter "Appellant") is Micron Technology, Inc., the assignee of the above-referenced application, as evidenced by the assignment recorded with the United States Patent and Trademark Office on January 9, 2005, at Reel 014856, Frame 0025.

(2) RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related applications that are on appeal or subject to other proceedings before the Board of Patent Appeals and Interferences, or of any other proceedings, that would influence or affect the decision of the Board of Patent Appeals and Interferences (hereinafter "the Board") in the above-referenced appeal.

(3) STATUS OF THE CLAIMS

Claims 1-14 and 25-39 are currently pending and under consideration in the above-referenced application. Each of claims 1-14 and 25-39 has been considered and stands rejected.

The rejections of claims 1-14 and 25-39 are being appealed.

(4) STATUS OF AMENDMENTS

No amendments have been proposed in the present application subsequent to the final rejection mailed October 10, 2006.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

While reference characters are used in the following summary to identify examples of claim elements that are shown in the drawings, it should be noted that the reference characters are included merely to ensure full compliance with the requirements of 37 C.F.R. § 41.37(c)(1)(v), and that their inclusion merely points to examples in the as-filed disclosure that do not limit the scope of any claim that remains pending in the above-referenced application. Rather, the scope of each claim is limited only by the plain language thereof, and includes the full scope of available equivalents to each recited element.

Independent claim 1 recites a method for supporting wafers for singulation and pick-and-place. With reference to FIGS. 1-4 of the presently considered application, the method of independent claim 1 includes providing a semiconductor wafer 10. (As filed Application, page 8, lines 9-12 (¶ [0023]); FIG. 1). The method further includes mounting an adhesive coated tape 22 to a surface of the semiconductor wafer 10. (*Id.*, page 10, lines 3-9, 19-28 (¶¶ [0026] and [0028]); FIGS. 2, 3A, and 4). The method further includes gripping the semiconductor wafer 10 along at least a portion of the periphery thereof. (*Id.*, page 11, lines 10-14 (¶ [0030]); FIG. 2). The method further includes singulating individual components 18 from the semiconductor wafer 10, leaving a ring of material 14/14P comprising at least in part a material of the semiconductor wafer 10 along the periphery thereof. (*Id.*, page 11, lines 20-27; page 12, lines 19-23 (¶¶ [0030]

and [0032]); FIGS. 2-4). Finally, the method includes removing at least some individual components 18 from the adhesive-coated tape 22. (*Id.*, page 11, line 28 – page 12, line 25 (¶¶ [0031] and [0032]); FIG. 4).

Independent claim 25 recites a method for processing a semiconductor device wafer. With reference to FIGS. 1-4 of the presently considered application, the method of independent claim 25 includes mounting an adhesive-coated tape 22 to a surface of a semiconductor wafer 10. (*Id.*, page 10, lines 3-9, 19-28 (¶¶ [0026] and [0028]); FIGS. 2, 3A, and 4). The method further includes singulating individual components 18 from the semiconductor wafer 10 and removing at least some singulated individual components 18 without using a film frame while the adhesive-coated tape 22 is mounted to the surface thereof. (*Id.*, page 11, lines 10-27 (¶ [0030]); FIG. 2).

Independent claim 29 recites a method of processing a semiconductor wafer. With reference to FIGS. 1-4 of the presently considered application, the method of independent claim 29 includes gripping a semiconductor wafer 10 along at least a portion of a periphery thereof. (*Id.*, page 11, lines 10-14 (¶ [0030]); FIG. 2). The method further includes singulating individual components 18 from the semiconductor wafer 10 while leaving an uncut peripheral ring of material 14/14P comprising at least in part a material of the semiconductor wafer 10 thereabout. (*Id.*, page 11, lines 20-27; page 12, lines 19-23 (¶¶ [0030] and [0032]); FIGS. 2-4).

Independent claim 38 recites a method of using a 300 mm semiconductor wafer 10, including handling the 300 mm semiconductor wafer 10 with equipment sized to handle 200 mm semiconductor wafers. (*Id.*, page 8, lines 18-21 (¶ [0024]); FIG. 1).

In regards to dependent claim 2, gripping the semiconductor wafer 10, may further include gripping the semiconductor wafer 10 by the ring of material 14/14P along at least a

portion of the periphery thereof during the removing of the at least some individual components. (*Id.*, page 10, lines 10-14 (¶ [0030]); FIG. 2).

In regards to dependent claims 4, 5, and 6, at least a portion of the ring of material 14/14P may be formed from a polymer material disposed about and contiguous with a periphery of the semiconductor wafer 10 and of thickness at least as great as a thickness of the semiconductor wafer 10. In addition, the ring of material 14/14P disposed about a periphery may be from a polymer material by one of spin-coating, stereolithography or molding. (*Id.*, page 8, line 22 – page 10, line 2 (¶ [0025]); FIG. 3A).

In regards to dependent claim 8, semiconductor wafer 10 may be singulated from a backside of wafer 10. (*Id.*, page 11, lines 5-8 (¶ [0030])).

In regards to dependent claim 12, a UV-sensitive adhesive 22 may be exposed prior to removing the at least some individual components 18 while leaving a portion on the adhesive-coated tape 22 extended over the ring of material unexposed. (*Id.*, page 10, lines 19-23 (¶ [0028]).

Claims 26-28 and 35-39 provide for handling a 300 mm semiconductor wafer 10 using equipment sized to handle a 200 mm semiconductor wafer. (*Id.*, page 8, lines 18-21 (¶ [0024]). Additionally, a 300 mm semiconductor wafer may be singulated using a 200 mm semiconductor wafer saw chuck. In addition, a 300 mm semiconductor wafer may be held in a 200 mm semiconductor wafer pick and place machine chuck while removing the at least some singulated individual components 18. (*Id.*, page 11, line 30 – page 12, line 1 (¶ [0031]).

Dependent claim 31 provides for gripping the uncut peripheral ring of material while removing the at least some singulated individual components 18 therefrom. (*Id.*, page 11, line 28 – page 12, line 15 (¶ [0031]).

Dependent claim 32 provides for defining an uncut peripheral ring of material from semiconductor material. (*Id.*, page 11, lines 3-27 (¶ [0030]).

Dependent claim 33 provides for defining an uncut peripheral ring of material at least in part from a polymer disposed about and contiguous with the semiconductor wafer. (*Id.*, page 11, lines 3-27 (¶ [0030])). (*Id.*, page 8, line 22 – page 10, line 2 (¶ [0025]); FIG. 3A);

Dependent claim 34 provides for defining the uncut peripheral ring of material in part from semiconductor material and in part from a polymer disposed about and contiguous with a periphery of the semiconductor wafer. (*Id.*, page 8, line 22 – page 10, line 2; (¶ [0025]); FIG. 3A);

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The 35 U.S.C. § 102(e) rejections of claims 1, 2, 4-14, 25, and 29-34 for being directed to subject matter which is allegedly anticipated by the subject matter described in U.S. Patent 6,680,241 to Okamoto et al. (hereinafter "Okamoto");

(B) The 35 U.S.C. § 103(a) rejection of claim 3 for being directed to subject matter which is allegedly unpatentable over the teachings of Okamoto in view of the teachings from Tandy et. al. (U.S. Patent Application Publication 2003/0003688).

(C) The 35 U.S.C. § 103(a) rejections of claims 26-28 and 35-39 for being directed to subject matter which is allegedly unpatentable over the teachings of Okamoto in view of the teachings from U.S. Patent 6,551,906 to Oka.

(7) ARGUMENT

(A) Rejections Under 35 U.S.C. § 102

Claims 1, 2, 4-14, 25, and 29-34 stand rejected under 35 U.S.C. § 102.

(1) Legal Authority

A claim is anticipated only if each and every element, as set forth in the claim, is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

(2) Reference Relied Upon

Okamoto

Okamoto discloses a method of improving the flexural strength of a chip by reducing the chipping and cracking of the chip that occurs during the processing of the chip. Col. 1, lines 35-39. In the method, a wafer sheet 2 is bonded to the front surface 1a of a 200 mm silicon wafer 1. Col. 2, lines 22-26; FIG. 1A. A grindstone 3 polishes the back surface 1b of the wafer 1. Col. 2, lines 26-27; FIG. 1A. Subsequently, a wafer sheet 5 is bonded to the back surface 1b of the

wafer 1. Col. 2, lines 37-38; FIG. 1C. A stainless steel frame 6 of a ring shape "physically supports the wafer sheet 5." Col. 2, lines 40-43; FIG. 1C. The wafer sheet 2 is removed from the wafer 1 and the wafer 1 is diced along scribe lines on the front surface 1a. Col. 2, lines 43-48; FIGS. 1C-1D. A wafer sheet 10 with a frame 11, apparently a stainless steel frame as described earlier with respect to frame 6, is applied to the front surface 1a and the wafer sheet 5 is removed. Col. 2, lines 48-51; FIG. 1D.

(3) Analysis

Claims 1, 2, 4-14, 25, and 29-34 stand rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by that described in Okamoto.

It is respectfully submitted that Okamoto does not expressly or inherently describe every element of independent claim 1. Specifically, Okamoto does not disclose a method that includes singulating components from a wafer and *leaving a ring of material that is comprised in part of the material from the wafer*. It is respectfully noted that the drawings disclose a wafer 1 bonded to a wafer sheet 5 that is supported by a stainless steel ring 6. Col. 2, lines 37-44; FIG. 1B. The wafer sheet, however, is not a part of the material of the semiconductor material. Rather, it is quite a distinct and separate item as Okamoto repeatedly states throughout the specification, a point, it is respectfully noted, that the Examiner apparently recognizes implicitly when describing the wafer sheet as "adhesive-coated tape." *See, e.g.*, Office Action of October 10, 2006, pg. 3. In addition, the Examiner takes the position that the wafer sheet 5 comprises the "ring of material." *Id.* at pg. 9. As described above, the wafer sheet 5 described in Okamoto is not part of the material of the wafer and, therefore, Okamoto does not describe leaving *a ring of material*

that is comprised in part of the material from the wafer.

As such, Okamoto does not expressly or inherently describe each and every element of independent claim 1.

Further, the withdrawal of the 35 U.S.C. § 102(e) rejections of claims 2 and 4-14 is respectfully requested as each claim depends either directly or indirectly from allowable independent claim 1, among other reasons.

Claim 2 is additionally allowable because Okamoto does not describe, expressly or inherently, gripping the semiconductor wafer by the ring of material (which, as recited in claim 1, includes a material of the semiconductor wafer) along at least a portion of the periphery thereof during the removing of the at least some individual components.

Claim 4 is additionally allowable because Okamoto does not describe, expressly or inherently, forming at least a portion of the ring of material from a polymer material disposed about and contiguous with a periphery of the semiconductor wafer and of thickness at least as great as a thickness of the semiconductor wafer. As discussed above, Okamoto does not disclose a ring of material formed from a wafer. Nor does Okamoto expressly or inherently disclose a ring of material formed from a polymer. Rather, Okamoto discloses a thin, reinforcing film 15 formed in a layer by spin coating. Col. 2, lines 65-67; Col. 3, lines 1-17; FIG. 1E. Additionally, as Okamoto notes, the polyimide film 15 is 10 μm or thinner as compared to post-backgrinding wafer thickness of 100 μm. Col. 4, lines 10-11, 17-20.

Claim 5 is additionally allowable because Okamoto does not describe, expressly or inherently, forming the ring in part from the material of the semiconductor wafer and in part from a polymer disposed about and contiguous with a periphery of the semiconductor wafer and of

thickness at least as great as a thickness of the semiconductor wafer, as discussed vis-à-vis claim 4.

Claim 6 is additionally allowable because Okamoto does not describe, expressly or inherently, forming the ring of material disposed about a periphery from a polymer material by one of spin-coating, stereolithography or molding. Okamoto disclose spin coating within the context of forming a uniform polyimide reinforcing film, not a ring of material, as discussed above vis-à-vis claim 4.

Claim 8 is additionally allowable because Okamoto does not describe, expressly or inherently, a method that includes singulating the semiconductor wafer from a backside of the wafer. Rather, Okamoto discloses dicing the wafer 1 along scribe lines formed on the front surface 1a of the wafer 1. Col. 2, lines 46-47; FIG. 1D.

Claim 12 is additionally allowable because Okamoto does not describe, expressly or inherently, a method that includes exposing a UV-sensitive adhesive prior to removing the at least some individual components while leaving a portion on the adhesive-coated tape extending over the ring of material unexposed. Rather, Okamoto describes applying ultraviolet rays to apparently the entire wafer sheet 10 so that the wafer sheet 10 may be removed from the chips 1c. Col. 3, lines 21-23; FIG. 1F.

It is respectfully submitted that Okamoto does not expressly or inherently describe every element of independent claim 25. Specifically, Okamoto does not disclose a method for processing a semiconductor wafer that includes singulating individual components from the semiconductor wafer...*without using a film frame while the adhesive-coated tape is mounted to*

the surface thereof. The disclosure of Okamoto is limited to using a stainless steel frame 6, 11, 21, 31, and 36. *See* FIGS. 1-5. Okamoto provides no indication of how the wafer sheets are supported beyond the frames and being set on the stage 54. The only indication that Okamoto provides that a film frame is unnecessary is during the formation of *grooves* 32 in the wafer 1. Col. 4, lines 51-55. In that instance, the silicon wafer 1 may have the grooves formed by "directly sucking it to a dicing stage, without bonding the wafer sheet 30. A wafer sheet without a frame may be used." Col. 4, lines 52-54; FIG. 3A. It is critical, however, that Okamoto immediately discloses using a wafer sheet 35 *with a frame* 36 for the subsequent grinding process which results in the singulation of chips 1c. Col. 4, lines 55-57; FIG. 3B.

As such, Okamoto does not expressly or inherently describe each and every element of independent claim 25.

It is respectfully submitted that Okamoto does not expressly or inherently describe every element of independent claim 29. As with independent claim 1 discussed above, Okamoto does not describe, expressly or inherentl,y a method of singulating individual components while leaving an uncut peripheral ring of material thereabout, as discussed above vis-à-vis independent claim 1.

The withdrawal of the 35 U.S.C. § 102(e) rejection of claims 30-34 is respectfully requested as each depends either directly or indirectly upon allowable independent claim 29, among other reasons.

Claim 31 is additionally allowable because Okamoto does not disclose gripping the uncut peripheral ring of material comprising at least in part a material of the semiconductor wafer while

removing the at least some singulated individual components. As discussed above, Okamoto discloses solely singulating and removing die components through the use of a wafer sheet frame.

Claim 32 is additionally allowable because Okamoto does not disclose defining an uncut peripheral ring of material from semiconductor material.

Claim 33 is additionally allowable because Okamoto does not disclose defining an uncut peripheral ring of material at least in part from a polymer disposed about and contiguous with the semiconductor wafer, as discussed above with respect to claim 4.

Claim 34 is additionally allowable because Okamoto does not disclose an uncut peripheral ring of material at least in part from semiconductor material and in part from a polymer disposed about and contiguous with the periphery of the semiconductor wafer, as discussed above with respect to claim 5.

Reversal of the 35 U.S.C. § 102 rejections of claims 1, 2, 4-14, 25, and 29-34 is respectfully requested.

(B) Rejections Under 35 U.S.C. § 103(a)

Claims 3, 26-28, and 35-39 stand rejected under 35 U.S.C. § 103(a).

(1) Legal Authority

The standard for establishing and maintaining a 35 U.S.C. § 103(a) rejection is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(2) Analysis

Okamoto in View of Tandy

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the subject matter taught in Okamoto, in view of the teachings of Tandy.

Claim 3 is allowable, among other reasons, for depending directly from independent claim 1, which is allowable.

Claim 3 is additionally allowable since neither Okamoto nor Tandy provides a suggestion or motivation to combine the references. Okamoto, as discussed above, relates to methods of using a wafer sheets and frames during a spin coating and singulating process. Tandy, conversely, relates to methods of marking semiconductor wafers and devices. The only apparent motivation to combine the references is improper hindsight based upon Appellant's own disclosure. Therefore, the withdrawal of the 35 U.S.C. § 103(a) obviousness rejection of dependent claim 3, is respectfully requested.

Okamoto in View of Oka

Claims 26-28 and 35-39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the subject matter taught in Okamoto, in view of the teachings of Oka.

Each of claims 26-28 are allowable, among other reasons, for depending directly or indirectly from independent claim 25, which is allowable.

Claim 26 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes handling a 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers. Rather, Oka teaches, in figures 1A-7H and corresponding text, a method of grinding a semiconductor wafer to desired *thickness* prior to singulation.

Claim 27 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck.

Claim 28 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components.

Each of claims 35-37 are allowable, among other reasons, for depending directly or indirectly from independent claim 29, which is allowable.

Claim 35 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes handling a 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers.

Claim 36 is additionally allowable because neither Okamoto nor Oka teaches or suggests

a method that includes singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck.

Claim 37 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components.

Independent claim 38 is allowable because neither Okamoto nor Oka teaches or suggests a method that includes handling a 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers, as discussed with respect to claims 26 and 28. Therefore, the withdrawal of the 35 U.S.C. § 103(a) rejection of independent claim 38 is respectfully requested.

Claim 39 is allowable, among other reasons, for depending directly or indirectly from independent claim 38, which is allowable.

Claim 39 is additionally allowable because neither Okamoto nor Oka teaches or suggests a method that includes processing the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers.

Further, neither Okamoto nor Oka provides a suggestion or motivation to combine the references. Okamoto, as discussed above, relates to methods of using a wafer sheets and frames during a spin coating and singulating process. Oka teaches a method of reducing the thickness of semiconductor wafers, not a method processing 300 mm semiconductor wafers on equipment sized to handle 200 mm wafers. Therefore, there is no motive or suggestion to combine Okamoto with Oka. The only apparent motivation to combine the references is improper hindsight based upon Appellant's own disclosure.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 103(a), the subject matter recited in claims 26-28 and 35-39 is allowable over the teachings of Okamoto and Oka.

(8) CLAIMS APPENDIX

A CLAIMS APPENDIX accompanies this APPEAL BRIEF and includes the most recent version of each claim that is still pending in the above-referenced application.

(9) EVIDENCE APPENDIX

No evidence is being submitted with this APPEAL BRIEF. Accordingly, there is no EVIDENCE APPENDIX to this APPEAL BRIEF.

(10) RELATED PROCEEDINGS APPENDIX

There are no decisions from related proceedings to file with this APPEAL BRIEF. Thus, there is no RELATED PROCEEDINGS APPENDIX to this APPEAL BRIEF.

(11) CONCLUSION

It is respectfully submitted that:

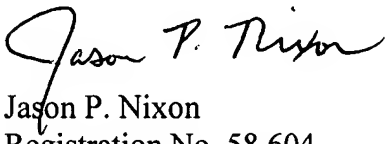
(A) Claims 1, 2, 4-14, 25 and 29-34 are allowable under 35 U.S.C. § 102(e) for reciting subject matter which is not anticipated by the subject matter described in Okamoto;

(B) Claim 3 is directed to subject matter that, under 35 U.S.C. § 103(a), is patentable over the subject matter taught in Okamoto, in view of teachings from Tandy; and

(C) Claims 26-28 and 35-39 are directed to subject matter that, under 35 U.S.C. § 103(a), is patentable over the subject matter taught in Okamoto, in view of teachings from Oka.

Accordingly, reversal of the rejections of claims 1-14 and 25-39 is respectfully requested, as is the allowance of each of these claims.

Respectfully submitted,



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April 12, 2007

JPN/jpn

Document in ProLaw

CLAIMS APPENDIX

1. A method for supporting wafers for singulation and pick-and-place, comprising:
providing a semiconductor wafer;
mounting an adhesive-coated tape to a surface of the semiconductor wafer;
gripping the semiconductor wafer along at least a portion of a periphery thereof;
singulating individual components from the semiconductor wafer, leaving a ring of material comprising at least in part a material of the semiconductor wafer along the periphery thereof; and
removing at least some individual components from the adhesive-coated tape.

2. The method of claim 1, wherein gripping the semiconductor wafer along at least a portion of the periphery thereof further includes gripping the semiconductor wafer by the ring of material during the removing of the at least some individual components.

3. The method of claim 1, further including forming the ring of material only from the material of the semiconductor wafer.

4. The method of claim 1, further including forming at least a portion of the ring of material from a polymer material disposed about and contiguous with a periphery of the semiconductor wafer and of thickness at least as great as a thickness of the semiconductor wafer.

5. The method of claim 1, further including forming the ring of material in part from the material of the semiconductor wafer and in part from a polymer disposed about and contiguous with a periphery of the semiconductor wafer and of thickness at least as great as a thickness of the semiconductor wafer.

6. The method of claim 5, further comprising forming the ring of material from the polymer material by one of spin-coating, stereolithography or molding.

7. The method of claim 1, further comprising backgrinding the semiconductor wafer

prior to singulation.

8. The method of claim 7, further comprising mounting the adhesive-coated tape to an active surface of the semiconductor wafer and singulating the semiconductor wafer from a backside thereof after backgrinding.

9. The method of claim 7, further comprising mounting the adhesive-coated tape to a backside of the semiconductor wafer and singulating the semiconductor wafer from an active surface thereof.

10. The method of claim 1, further comprising mounting the adhesive-coated tape to a backside of the semiconductor wafer and singulating the semiconductor wafer from an active surface thereof.

11. The method of claim 1, wherein mounting the adhesive-coated tape comprises mounting a tape bearing a UV-sensitive adhesive thereon.

12. The method of claim 11, further comprising exposing the UV-sensitive adhesive prior to removing the at least some individual components while leaving a portion on the adhesive-coated tape extending over the ring of material unexposed.

13. The method of claim 1, wherein the semiconductor wafer is singulated using one of laser cutting, water cutting and sawing.

14. The method of claim 1, further comprising discarding the ring of material, any remaining individual components and the adhesive-coated tape after removing the at least some individual components.

25. A method for processing a semiconductor wafer, comprising:
mounting an adhesive-coated tape to a surface of a semiconductor wafer; and
singulating individual components from the semiconductor wafer and removing at least some singulated individual components without using a film frame while the adhesive-coated tape is mounted to the surface thereof.

26. The method of claim 25, wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers.

27. The method of claim 26, further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck.

28. The method of claim 26, further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom.

29. A method of processing a semiconductor wafer, comprising:
gripping a semiconductor wafer along at least a portion of a periphery thereof; and
singulating individual components from the semiconductor wafer while leaving an uncut peripheral ring of material comprising at least in part a material of the semiconductor wafer thereabout.

30. The method of claim 29, further including removing at least some singulated individual components therefrom.

31. The method of claim 30, wherein gripping a semiconductor wafer along at least a portion of a periphery thereof further includes gripping the uncut peripheral ring of material while removing the at least some singulated individual components therefrom.

32. The method of claim 29, further comprising defining the uncut peripheral ring of material from semiconductor material.

33. The method of claim 29, further comprising defining the uncut peripheral ring of material at least in part from a polymer disposed about and contiguous with the semiconductor wafer.

34. The method of claim 29, further comprising defining the uncut peripheral ring of material in part from semiconductor material and in part from a polymer disposed about and contiguous with a periphery of the semiconductor wafer.

35. The method of claim 30, wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers.

36. The method of claim 35, further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck.

37. The method of claim 35, further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom.

38. A method of using a 300 mm semiconductor wafer, including handling the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers.

39. The method of claim 38, further including processing the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers.